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SYSTEM AND METHOD TO REDUCE NOISE IN A SUBSTRATE

CROSS-REFERENCE TO RELATED APPLICATIONS/INCORPORATION BY REFERENCE

AC 5/18/05

[01] This application is a continuation of United States Application Serial No. 10/294,880 filed on November 14, 2002, (Patent No. 6,870,228) which makes reference to, claims priority to and claims the benefit of United States Provisional Patent Application Serial No. 60/402,095 filed on August 7, 2002, and claims the benefit of United States Provisional Patent Application Serial No. 60/402,090 Filed on August 9, 2002.

[02] All of the above stated applications are incorporated herein by reference in their entirety.

FIELD OF THE INVENTION

[03] Certain embodiments of the invention relate to integrated circuit (IC) designs. More specifically, certain embodiments of the invention relate to a system for reducing noise in a substrate of an integrated circuit.

BACKGROUND OF THE INVENTION

[04] As more and more functional blocks are added, for example, to a chip, an integrated circuit (IC) or an integrated system or device, the risk for the generation and propagation of noise between the different functional blocks or within a functional block may become quite substantial.

[05] An exemplary conventional complementary metal oxide semiconductor (CMOS) transistor arrangement is illustrated in FIG. 1. As shown in FIG. 1, the conventional CMOS transistor arrangement 10 includes an n-channel MOS (NMOS) transistor 30 and a p-channel MOS (PMOS) transistor 40. The conventional CMOS arrangement 10 also includes a p-substrate 20 (e.g., a p^--substrate). The NMOS transistor 30 is disposed in the p-substrate 20. The NMOS transistor 30 includes a p^+-body (B), an n^+-source (S)